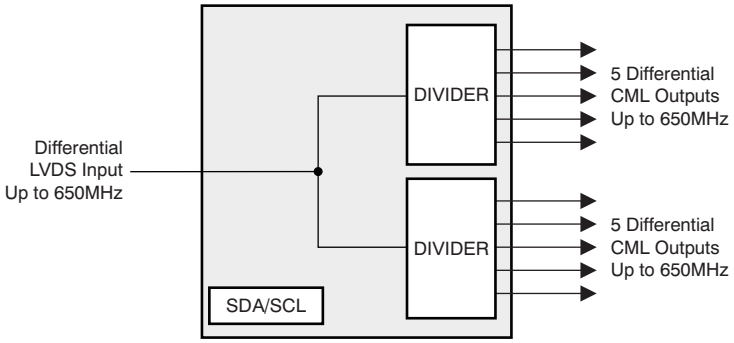
1.8V, 10 Output, High-Performance Clock Distributor

FEATURES

- Single 1.8V Supply
- High-Performance Clock Distributor with 10 Outputs
- Low Input-to-Output Additive Jitter: As Low As 10fs RMS
- Output Group Phase Adjustment
- Low-Voltage Differential Signaling (LVDS) Input, 100Ω Differential On-Chip Termination, Up to 650MHz Frequency
- Differential Current Mode Logic (CML) Outputs, 50Ω Single-Ended On-Chip Termination, Up to 650MHz Frequency
- Two Groups of Five Outputs Each with Independent Frequency Division Ratios
- Output Frequency Derived with Divide Ratios of 1, 2, 4, 5, 8, 10, 16, 20, 32, 40, and 80
- Meets ANSI TIA/EIA-644-A-2001 LVDS Standard Requirements
- Power Consumption: 410mW Typical
- Output Enable Control for Each Output
- SDA/SCL Device Management Interface
- 48-pin QFN (RGZ) Package
- Industrial Temperature Range: –40°C to +85°C

APPLICATIONS

- Clock Synthesis and Distribution for High-Speed SERDES
- Synthesis and Distribution of SERDES Reference Clocks for 1G/10G Ethernet, 1X/2X/4X/10X Fibre Channel, PCI Express, Serial ATA, SONET, CPRI, OBSAI, etc.
- Up to 1-to-10 Clock Buffering and Fan-out



DESCRIPTION

The CDCL1810 is a high-performance clock distributor. The programmable dividers, P0 and P1, give a high flexibility to the ratio of the output frequency to the input frequency:

$$F_{OUT} = F_{IN}/P$$

Where:

P (P0,P1) = 1, 2, 4, 5, 8, 10, 16, 20, 32, 40, 80

The CDCL1810 supports one differential LVDS clock input and a total of 10 differential CML outputs. The CML outputs are compatible with LVDS receivers if they are ac-coupled.

With careful observation of the input voltage swing and common-mode voltage limits, the CDCL1810 can support a single-ended clock input as outlined in the Pin Description Table.

All device settings are programmable through the SDA/SCL, serial two-wire interface.

The phase of one output group relative to the other can be adjusted through the SDA/SCL interface. For post-divide ratios (P0, P1) that are multiples of 5, the total number of phase adjustment steps (*n*) equals the divide-ratio divided by 5. For post-divide ratios (P0, P1) that are not multiples of 5, the total number of steps (*n*) is the same as the post-divide ratio. The phase adjustment step ($\Delta\Phi$) in time units is given as:

$$\Delta\Phi = 1/(n \times F_{OUT})$$

where F_{OUT} is the respective output frequency.

The device operates in a 1.8V supply environment and is characterized for operation from –40°C to +85°C. The CDCL1810 is available in a 48-pin QFN (RGZ) package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS(1)

T_A	PACKAGED DEVICES	FEATURES
–40°C to +85°C	CDCL1810RGZT	48-pin QFN (RGZ) Package, small tape and reel
–40°C to +85°C	CDCL1810RGZR	48-pin QFN (RGZ) Package, tape and reel

(1) For the most current specifications and package information, see the Package Option Addendum located at the end of this data sheet or refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE	UNIT
V_{DD}, AV_{DD}	Supply voltage(2)	–0.3 to 2.5	V
V_{LVDS}	Voltage range at LVDS input pins(2)	–0.3 to 4.0	V
V_I	Voltage range at all non-LVDS input pins(2)	–0.3 to 3.0	V
ESD	Electrostatic discharge (HBM)	2	kV
T_J	Junction temperature	+125	°C
T_{STG}	Storage temperature range	–65 to +150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating condition* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{DD}	Digital supply voltage	1.7	1.8	1.9	V
AV_{DD}	Analog supply voltage	1.7	1.8	1.9	V
T_A	Ambient temperature (no airflow, no heatsink)	–40		+85	°C
T_J	Junction temperature			+105	°C
θ_{JA}	Junction-to-ambient thermal resistance(1):				°C/W
	airflow = 0 lfm		28.3		
	airflow = 50 lfm		22.4		

(1) No heatsink; power uniformly distributed; 36 ground vias (6 x 6 array) tied to the thermal exposed pad; 4-layer high-K board.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD}	Total current from digital 1.8V supply	All outputs enabled; $V_{DD} = V_{DD,typ}$ 650MHz LVDS input		212		mA
I_{AVDD}	Total current from analog 1.8V supply	All outputs enabled; $AV_{DD} = V_{DD,typ}$ 650MHz LVDS input		16		mA
$V_{IL,CMOS}$	Low level CMOS input voltage	V_{DD} = 1.8V	–0.2		0.6	V
$V_{IH,CMOS}$	High level CMOS input voltage	V_{DD} = 1.8V	V_{DD} –0.6		V_{DD}	V
$I_{IL,CMOS}$	Low level CMOS input current	$V_{DD} = V_{DD,max}$, V_{IL} = 0.0V			–120	µA
$I_{IH,CMOS}$	High level CMOS input current	$V_{DD} = V_{DD,max}$, V_{IH} = 1.9V			65	µA
$V_{OL,SDA}$	Low level CMOS output voltage for the SDA pin	Sink current = 3 mA	0		$0.2V_{DD}$	V
$I_{OL,CMOS}$	Low level CMOS output current				8	mA

AC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Z_{D,IN}$	Differential input impedance for the LVDS input terminals		90		132	Ω
$V_{CM,IN}$	Common-mode voltage, LVDS input		1125	1200	1375	mV
$V_{S,IN}$	Single-ended LVDS input voltage swing		100		600	mV_{PP}
$V_{D,IN}$	Differential LVDS input voltage swing		200		1200	mV_{PP}
$t_{R,OUT}$, $t_{F,OUT}$	Output signal rise/fall time	20%–80%		100		ps
$V_{CM,OUT}$	Common-mode voltage, CML outputs		V_{DD} – 0.31	V_{DD} – 0.23	V_{DD} – 0.19	V
$V_{S,OUT}$	Single-ended CML output voltage swing	ac-coupled	180	230	280	mV_{PP}
$V_{D,OUT}$	Differential CML output voltage swing	ac-coupled	360	460	560	mV_{PP}
F_{IN}	Clock input frequency				650	MHz
F_{OUT}	Clock output frequency				650	MHz

AC ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
J_{OUT}	Additive clock output jitter	F_{IN} = 30.72MHz, F_{OUT} = 30.72MHz $V_{D,IN}$ = 200mV_{PP}				
		10Hz–1MHz offset		188		fs RMS
		1MHz–5MHz offset		480		fs RMS
		12kHz–5MHz offset		514		fs RMS
		F_{IN} = 30.72MHz, F_{OUT} = 30.72MHz $V_{D,IN}$ = 1200mV_{PP}				
		10Hz–1MHz offset		257		fs RMS
		1MHz–5MHz offset		500		fs RMS
		12kHz–5MHz offset		570		fs RMS
		F_{IN} = 650MHz, F_{OUT} = 650MHz $V_{D,IN}$ = 200mV_{PP}				
		10Hz–1MHz offset		27		fs RMS
		1MHz–20MHz offset		66		fs RMS
		12kHz–20MHz offset		72		fs RMS
		F_{IN} = 650MHz, F_{OUT} = 650MHz $V_{D,IN}$ = 1200mV_{PP}				
		10Hz–1MHz offset		12		fs RMS
		1MHz–20MHz offset		23		fs RMS
		12kHz–20MHz offset		27		fs RMS
T_P	Input-to-output delay	F_{IN} = 30.72MHz, F_{OUT} = 30.72MHz YP[9:0] outputs		3		ns
TS_{OUT}	Clock output skew	F_{IN} = 30.72MHz, F_{OUT} = 30.72MHz YP[9:0] outputs relative to YP[0]	–64		64	ps

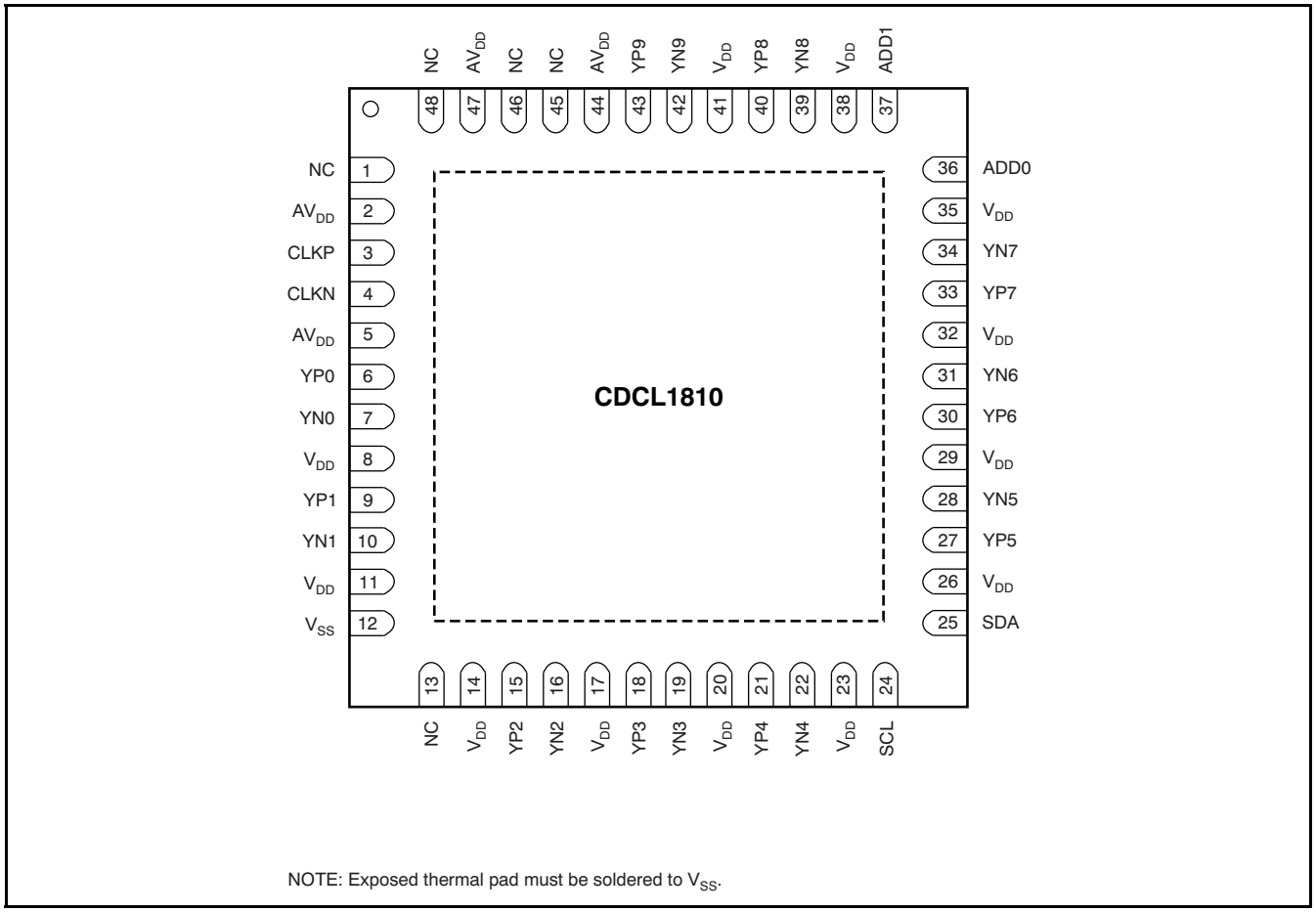
AC ELECTRICAL CHARACTERISTICS FOR THE SDA/SCL INTERFACE(1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCL}	SCL frequency			400	kHz
$t_{h(START)}$	START hold time	0.6			µs
$t_{w(SCLL)}$	SCL low-pulse duration	1.3			µs
$t_{w(SCLH)}$	SCL high-pulse duration	0.6			µs
$t_{su(START)}$	START setup time	0.6			µs
$t_{h(SDATA)}$	SDA hold time	0			µs
$t_{su(DATA)}$	SDA setup time	0.6			µs
$t_{r(SDATA)}$	SCL / SDA input rise time			0.3	µs
$t_{f(SDATA)}$	SCL / SDA input fall time			0.3	µs
$t_{su(STOP)}$	STOP setup time	0.6			µs
t_{BUS}	bus free time	1.3			µs

(1) See Figure 3 for the timing behavior.

DEVICE INFORMATION

48-PIN QFN (RGZ)
(TOP VIEW)



NOTE: Exposed thermal pad must be soldered to V_{SS}.

The CDCL1810 is available in a 48-pin QFN (RGZ) package with a pin pitch of 0,5mm. The exposed thermal pad serves both thermal and electrical grounding purposes.

NOTE:

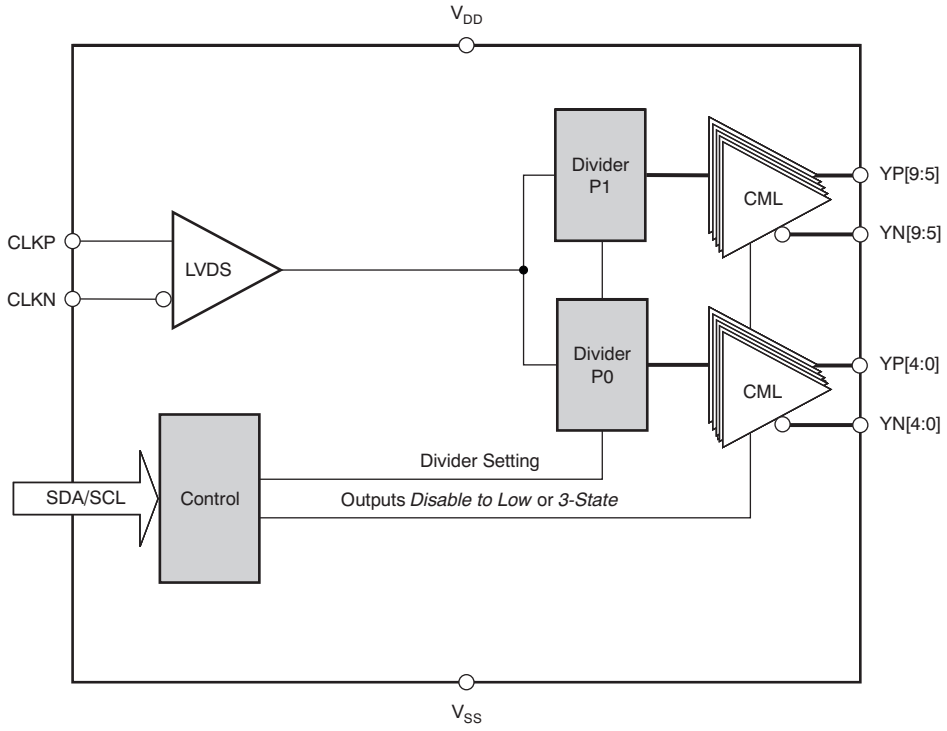
The device must be soldered to ground (V_{SS}) using as many ground vias as possible. The device performance will be severely impacted if the exposed thermal pad is not grounded appropriately.

DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	PIN NO.		
V_{DD}	8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41	Power	1.8V digital power supply.
AV_{DD}	2, 5, 44, 47	Power	1.8V analog power supply.
V_{SS}	Exposed thermal pad and pin 12	Power	Ground reference.
NC	1, 13, 45, 46, 48	I	Not connected; leave open.
CLKP, CLKN	3, 4	I	Differential LVDS input. Single-ended 1.8-V input can be dc-coupled to pin 3 with pin 4 either tied to pin 3 (recommended) or left open.
YP0, YN0 YP1, YN1 YP2, YN2 YP3, YN3 YP4, YN4 YP5, YN5 YP6, YN6 YP7, YN7 YP8, YN8 YP9, YN9	6, 7 9, 10 15, 16 18, 19 21, 22 27, 28 30, 31 33, 34 40, 39 43, 42	O	10 differential CML outputs.
SCL	24	I	SDA/SCL serial clock pin. Open drain. Always connect to a pull-up resistor.
SDA	25	I/O	SDA/SCL bidirectional serial data pin. Open drain. Always connect to a pull-up resistor.
ADD1, ADD0	37, 36	I	Configurable least significant bits (ADD[1:0]) of the SDA/SCL device address. The fixed most significant bits (ADD[6:2]) of the 7-bit device address are 11010.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Typical operating conditions are at V_{DD} = 1.8V and T_A = +25°C, $V_{D,IN}$ = 200mV_{PP} (unless otherwise noted).

TRANSIENT PERFORMANCE:
F_{IN} = 30.72MHz, F_{OUT} = 30.72MHz

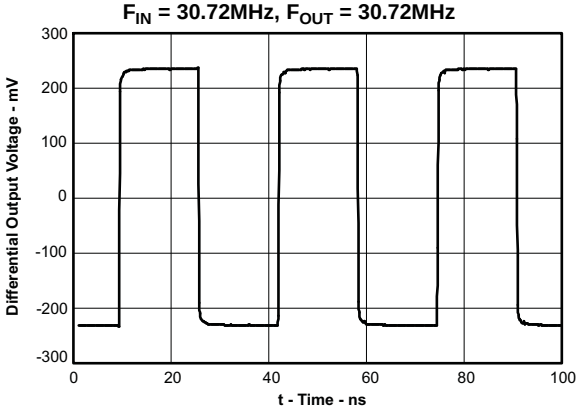


Figure 1.

TRANSIENT PERFORMANCE:
F_{IN} = 650MHz, F_{OUT} = 650MHz

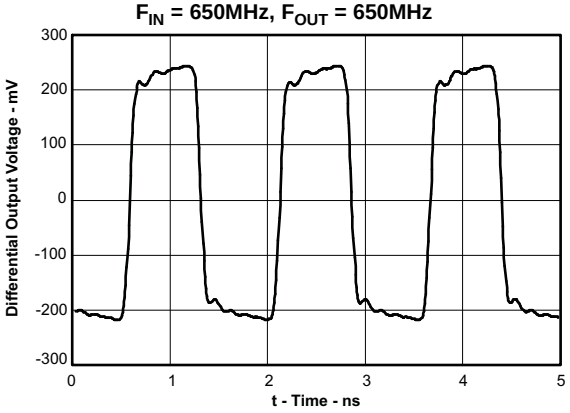


Figure 2.

SDA/SCL INTERFACE

This section describes the SDA/SCL interface of the CDCL1810 device. The CDCL1810 operates as a slave device of the industry standard 2-pin SDA/SCL bus. It operates in the fast-mode at a bit-rate of up to 400 kbit/s and supports 7-bit addressing compatible with the popular 2-pin serial interface standard.

SDA/SCL Bus Slave Device Address

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	ADD1	ADD0	0/1

The device address is made up of the fixed internal address, 11010 (A6:A2), and configurable external pins ADD1 (A1) and ADD0 (A0). Four different devices with addresses 1101000, 1101001, 1101010 and 1101011, can be addressed via the same SDA/SCL bus interface. The least significant bit of the address byte designates a write or read operation.

R/W Bit:

0 = write to CDCL1810 device

1 = read from CDCL1810 device

Command Code Definition

BIT	DESCRIPTION
C7	1 = *Byte Write* / *Read* or *Word Write* / *Read* operation
(C6:C0)	Byte Offset for *Byte Write* / *Read* and *Word Write* / *Read* operation.

Command Code for *Byte Write* / *Read* Operation	**Hex Code**	**C7**	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**
byte 0	80h	1	0	0	0	0	0	0	0
byte 1	81h	1	0	0	0	0	0	0	1
byte 2	82h	1	0	0	0	0	0	1	0
byte 3	83h	1	0	0	0	0	0	1	1
byte 4	84h	1	0	0	0	0	1	0	0
byte 5	85h	1	0	0	0	0	1	0	1
byte 6	86h	1	0	0	0	0	1	1	0

Command Code for *Word Write* / *Read* Operation	**Hex Code**	**C7**	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**
word 0: byte 0 and byte 1	80h	1	0	0	0	0	0	0	0
word 1: byte 1 and byte 2	81h	1	0	0	0	0	0	0	1
word 2: byte 2 and byte 3	82h	1	0	0	0	0	0	1	0
word 3: byte 3 and byte 4	83h	1	0	0	0	0	0	1	1
word 4: byte 4 and byte 5	84h	1	0	0	0	0	1	0	0
word 5: byte 5 and byte 6	85h	1	0	0	0	0	1	0	1
word 6: byte 6 and byte 7	86h	1	0	0	0	0	1	1	0

SDA/SCL Timing Characteristics

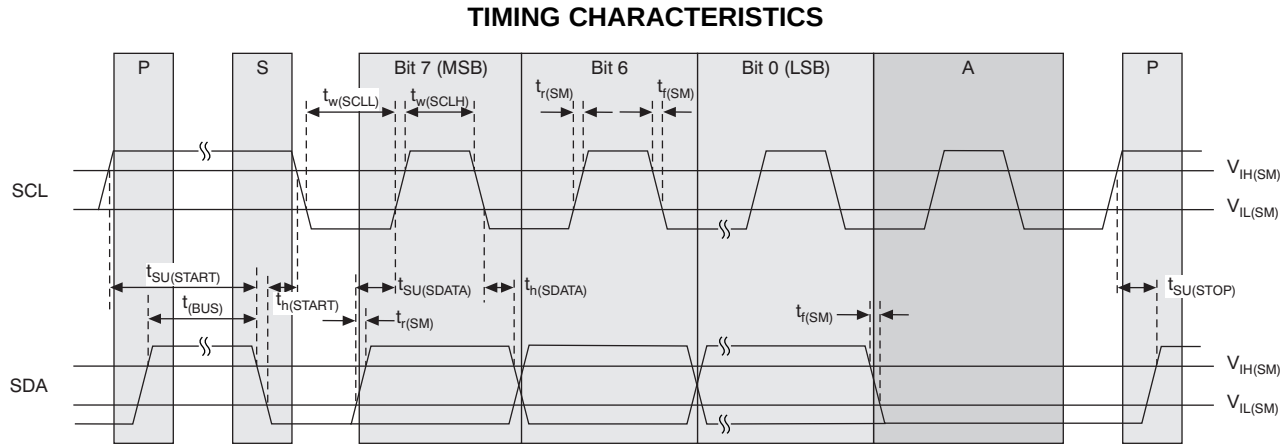
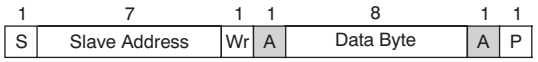


Figure 3. Timing Diagram for the SDA/SCL Serial Control Interface

SDA/SCL Programming Sequence

LEGEND FOR PROGRAMMING SEQUENCE



S	Start condition
Sr	Repeated start condition
Rd	Read (bit value = 1)
Wr	Write (bit value = 0)
A	Acknowledge (bit value = 0)
N	Not acknowledge (bit value = 1)
P	Stop condition
	Master to Slave transmission
	Slave to Master transmission

Byte Write Programming Sequence:

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	P

Byte Read Programming Sequence:

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	N	P

Word Write Programming Sequence:

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P

Word Read Programming Sequence:

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	A	Data Byte	N	P

SDA/SCL Bus Configuration Command Bitmap

Byte 0:

Bit	Bit Name	Description/Function	Type	Power Up Condition	Reference To
7	MANF[7]	Manufacturer reserved	R		
6	MANF[6]	Manufacturer reserved	R		
5	MANF[5]	Manufacturer reserved	R		
4	MANF[4]	Manufacturer reserved	R		
3	MANF[3]	Manufacturer reserved	R		
2	MANF[2]	Manufacturer reserved	R		
1	MANF[1]	Manufacturer reserved	R		
0	MANF[0]	Manufacturer reserved	R		

Byte 1:

Bit	Bit Name	Description/Function	Type	Power Up Condition	Reference To
7	RES	Reserved	R/W	0	
6	RES	Reserved	R/W	0	
5	ENPH	Phase select enable	R/W	1	
4	PH1[4]	Phase select for YP[9:5] and YN[9:5]	R/W	0	Table 2, Table 3
3	PH1[3]	Phase select for YP[9:5] and YN[9:5]	R/W	0	Table 2, Table 3
2	PH1[2]	Phase select for YP[9:5] and YN[9:5]	R/W	0	Table 2, Table 3
1	PH1[1]	Phase select for YP[9:5] and YN[9:5]	R/W	0	Table 2, Table 3
0	PH1[0]	Phase select for YP[9:5] and YN[9:5]	R/W	0	Table 2, Table 3

Byte 2:

Bit	Bit Name	Description/Function	Type	Power Up Condition	Reference To
7	RES	Reserved	R/W	0	
6	RES	Reserved	R/W	0	
5	ENP1	Post-divider P1 enable; if 0 output YP[9:5] and YN[9:5] are disabled	R/W	1	
4	RES	Reserved	R/W	1	
3	SELP1[3]	Divide ratio select for post-divider P1	R/W	0	Table 1
2	SELP1[2]	Divide ratio select for post-divider P1	R/W	0	Table 1
1	SELP1[1]	Divide ratio select for post-divider P1	R/W	0	Table 1
0	SELP1[0]	Divide ratio select for post-divider P1	R/W	0	Table 1

Byte 3:

Bit	Bit Name	Description/Function	Type	Power Up Condition	Reference To
7	RES	Reserved	R/W	0	
6	RES	Reserved	R/W	0	
5	RES	Reserved	R/W	0	
4	PH0[4]	Phase select for YP[4:0] and YN[4:0]	R/W	0	Table 2, Table 3
3	PH0[3]	Phase select for YP[4:0] and YN[4:0]	R/W	0	Table 2, Table 3
2	PH0[2]	Phase select for YP[4:0] and YN[4:0]	R/W	0	Table 2, Table 3
1	PH0[1]	Phase select for YP[4:0] and YN[4:0]	R/W	0	Table 2, Table 3
0	PH0[0]	Phase select for YP[4:0] and YN[4:0]	R/W	0	Table 2, Table 3

Byte 4:

Bit	Bit Name	Description/Function	Type	Power Up Condition	Reference To
7	RES	Reserved	R/W	0	
6	RES	Reserved	R/W	0	
5	ENP0	Post-divider P0 enable. If 0, output YP[4:0] and YN[4:0] are disabled	R/W	1	
4	RES	Reserved	R/W	1	
3	SELP0[3]	Divide ratio select for post-divider P0	R/W	0	Table 1
2	SELP0[2]	Divide ratio select for post-divider P0	R/W	0	Table 1
1	SELP0[1]	Divide ratio select for post-divider P0	R/W	0	Table 1
0	SELP0[0]	Divide ratio select for post-divider P0	R/W	0	Table 1

Byte 5:

Bit	Bit Name	Description/Function	Type	Power Up Condition	Reference To
7	EN	Chip enable; if 0 chip is in Iddq mode	R/W	1	
6	RES	Reserved	R	1	
5	ENDRV9	YP[9], YN[9] enable; if 0 output is disabled	R/W	1	
4	ENDRV8	YP[8], YN[8] enable; if 0 output is disabled	R/W	1	
3	ENDRV7	YP[7], YN[7] enable; if 0 output is disabled	R/W	1	
2	ENDRV6	YP[6], YN[6] enable; if 0 output is disabled	R/W	1	
1	ENDRV5	YP[5], YN[5] enable; if 0 output is disabled	R/W	1	
0	ENDRV4	YP[4], YN[4] enable; if 0 output is disabled	R/W	1	

Byte 6:

Bit	Bit Name	Description/Function	Type	Power Up Condition	Reference To
7	ENDRV3	YP[3], YN[3] enable; if 0 output is disabled	R/W	1	
6	ENDRV2	YP[2], YN[2] enable; if 0 output is disabled	R/W	1	
5	ENDRV1	YP[1], YN[1] enable; if 0 output is disabled	R/W	1	
4	ENDRV0	YP[0], YN[0] enable; if 0 output is disabled	R/W	1	
3	RES	Reserved	R/W	0	
2	RES	Reserved	R/W	0	
1	RES	Reserved	R/W	0	
0	RES	Reserved	R/W	0	

Table 1. Divide Ratio Settings for Post-Divider P0 or P1

Divide Ratio	SELP1[3] or SELP0[3]	SELP1[2] or SELP0[2]	SELP1[1] or SELP0[1]	SELP1[0] or SELP0[0]	Notes
1	0	0	0	0	Default
2	0	0	0	1	
4	0	0	1	0	
5	0	0	1	1	
8	0	1	0	0	
10	0	1	0	1	
16	0	1	1	0	
20	0	1	1	1	
32	1	0	0	0	
40	1	0	0	1	
80	1	0	1	0	

Table 2. Phase Settings for Divide Ratio = 5, 10, 20, 40, 80

Divide Ratio	With PH0[4:0] = 00000					Phase Lead (radian)	Notes
	PH1						
	[4]	[3]	[2]	[1]	[0]		
5	X	X	X	X	X	0	Phase setting not available
10	X	X	X	0	X	0	
	X	X	X	1	X	(2π/2)	
20	X	X	0	0	X	0	
	X	X	0	1	X	(2π/4)	
	X	X	1	0	X	2(2π/4)	
	X	X	1	1	X	3(2π/4)	
40	X	0	0	0	X	0	
	X	0	0	1	X	(2π/8)	
	X	0	1	0	X	2(2π/8)	
	X	0	1	1	X	3(2π/8)	
	X	1	0	0	X	4(2π/8)	
	X	1	0	1	X	5(2π/8)	
	X	1	1	0	X	6(2π/8)	
	X	1	1	1	X	7(2π/8)	

Table 2. Phase Settings for Divide Ratio = 5, 10, 20, 40, 80 (continued)

Divide Ratio	With PH0[4:0] = 00000					Phase Lead (radian)	Notes
	PH1						
	[4]	[3]	[2]	[1]	[0]		
80	0	0	0	0	X	0	
	0	0	0	1	X	(2π/16)	
	0	0	1	0	X	2(2π/16)	
	0	0	1	1	X	3(2π/16)	
	0	1	0	0	X	4(2π/16)	
	0	1	0	1	X	5(2π/16)	
	0	1	1	0	X	6(2π/16)	
	0	1	1	1	X	7(2π/16)	
	1	0	0	0	X	8(2π/16)	
	1	0	0	1	X	9(2π/16)	
	1	0	1	0	X	10(2π/16)	
	1	0	1	1	X	11(2π/16)	
	1	1	0	0	X	12(2π/16)	
	1	1	0	1	X	13(2π/16)	
	1	1	1	0	X	14(2π/16)	
	1	1	1	1	X	15(2π/16)	

Table 3. Phase Settings for Divide Ratio = 1, 2, 4, 8, 16, 32

Divide Ratio	With PH0[4:0] = 00000 PH1 [4]	[3]	[2]	[1]	[0]	Phase Lead (radian)	Notes
1	X	X	X	X	X	0	00000: Default Phase setting not available
2	X	X	X	X	0	0	
	X	X	X	X	1	(2π/2)	
4	X	X	X	0	0	0	
	X	X	X	0	1	(2π/4)	
	X	X	X	1	0	2(2π/4)	
	X	X	X	1	1	3(2π/4)	
8	X	X	0	0	0	0	
	X	X	0	0	1	(2π/8)	
	X	X	0	1	0	2(2π/8)	
	X	X	0	1	1	3(2π/8)	
	X	X	1	0	0	4(2π/8)	
	X	X	1	0	1	5(2π/8)	
	X	X	1	1	0	6(2π/8)	
	X	X	1	1	1	7(2π/8)	
16	X	0	0	0	0	0	
	X	0	0	0	1	(2π/16)	
	X	0	0	1	0	2(2π/16)	
	X	0	0	1	1	3(2π/16)	
	X	0	1	0	0	4(2π/16)	
	X	0	1	0	1	5(2π/16)	
	X	0	1	1	0	6(2π/16)	
	X	0	1	1	1	7(2π/16)	
	X	1	0	0	0	8(2π/16)	
	X	1	0	0	1	9(2π/16)	
	X	1	0	1	0	10(2π/16)	
	X	1	0	1	1	11(2π/16)	
	X	1	1	0	0	12(2π/16)	
	X	1	1	0	1	13(2π/16)	
	X	1	1	1	0	14(2π/16)	
	X	1	1	1	1	15(2π/16)	

Table 3. Phase Settings for Divide Ratio = 1, 2, 4, 8, 16, 32 (continued)

Divide Ratio	With PH0[4:0] = 00000					Phase Lead (radian)	Notes
	PH1						
	[4]	[3]	[2]	[1]	[0]		
32	0	0	0	0	0	0	
	0	0	0	0	1	(2π/32)	
	0	0	0	1	0	2(2π/32)	
	0	0	0	1	1	3(2π/32)	
	0	0	1	0	0	4(2π/32)	
	0	0	1	0	1	5(2π/32)	
	0	0	1	1	0	6(2π/32)	
	0	0	1	1	1	7(2π/32)	
	0	1	0	0	0	8(2π/32)	
	0	1	0	0	1	9(2π/32)	
	0	1	0	1	0	10(2π/32)	
	0	1	0	1	1	11(2π/32)	
	0	1	1	0	0	12(2π/32)	
	0	1	1	0	1	13(2π/32)	
	0	1	1	1	0	14(2π/32)	
	0	1	1	1	1	15(2π/32)	
	1	0	0	0	0	16(2π/32)	
	1	0	0	0	1	17(2π/32)	
	1	0	0	1	0	18(2π/32)	
	1	0	0	1	1	19(2π/32)	
	1	0	1	0	0	20(2π/32)	
	1	0	1	0	1	21(2π/32)	
	1	0	1	1	0	22(2π/32)	
	1	0	1	1	1	23(2π/32)	
	1	1	0	0	0	24(2π/32)	
	1	1	0	0	1	25(2π/32)	
	1	1	0	1	0	26(2π/32)	
	1	1	0	1	1	27(2π/32)	
	1	1	1	0	0	28(2π/32)	
	1	1	1	0	1	29(2π/32)	
	1	1	1	1	0	30(2π/32)	
	1	1	1	1	1	31(2π/32)	

PACKAGING INFORMATION

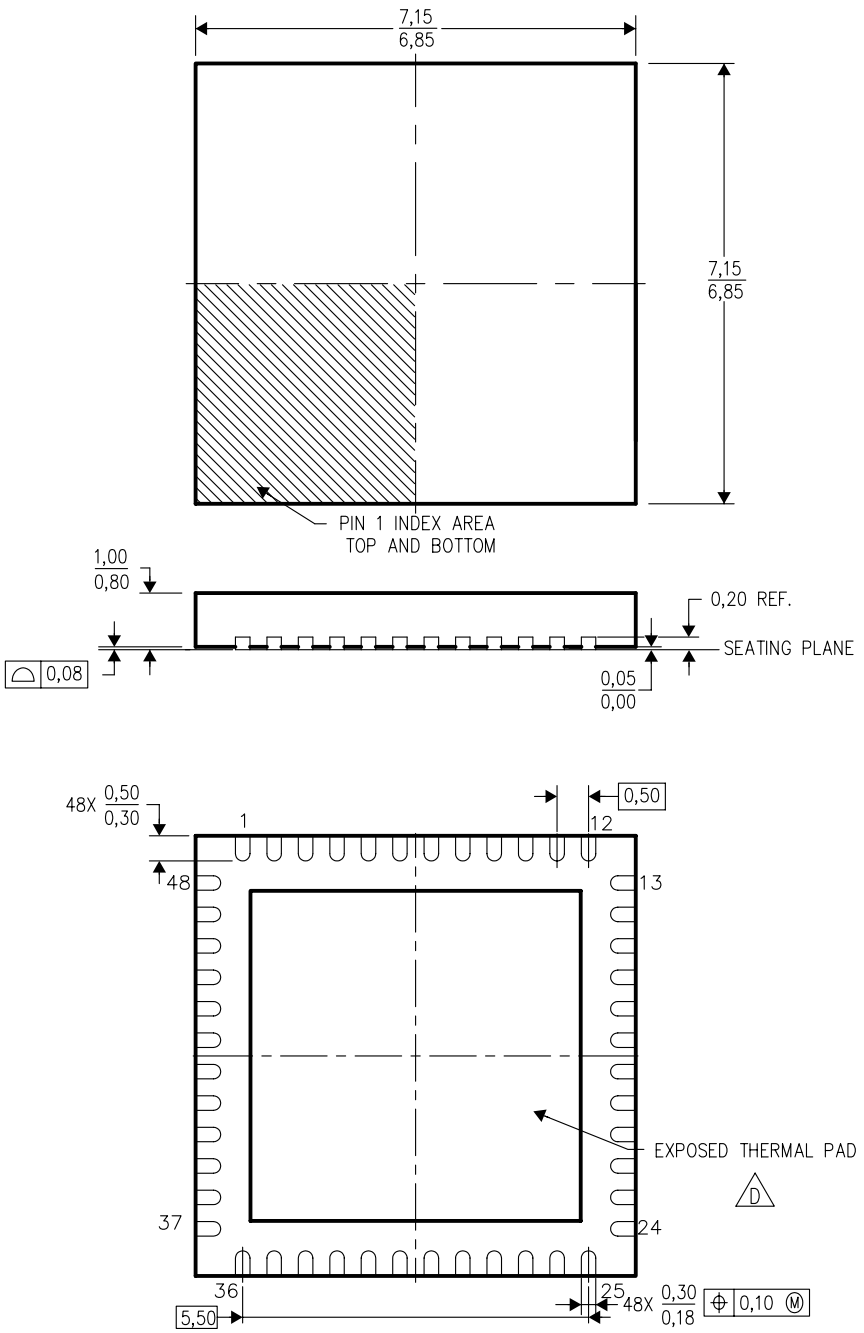
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CDCL1810RGZR	ACTIVE	QFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
CDCL1810RGZRG4	ACTIVE	QFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
CDCL1810RGZT	ACTIVE	QFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
CDCL1810RGZTG4	ACTIVE	QFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RGZ (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

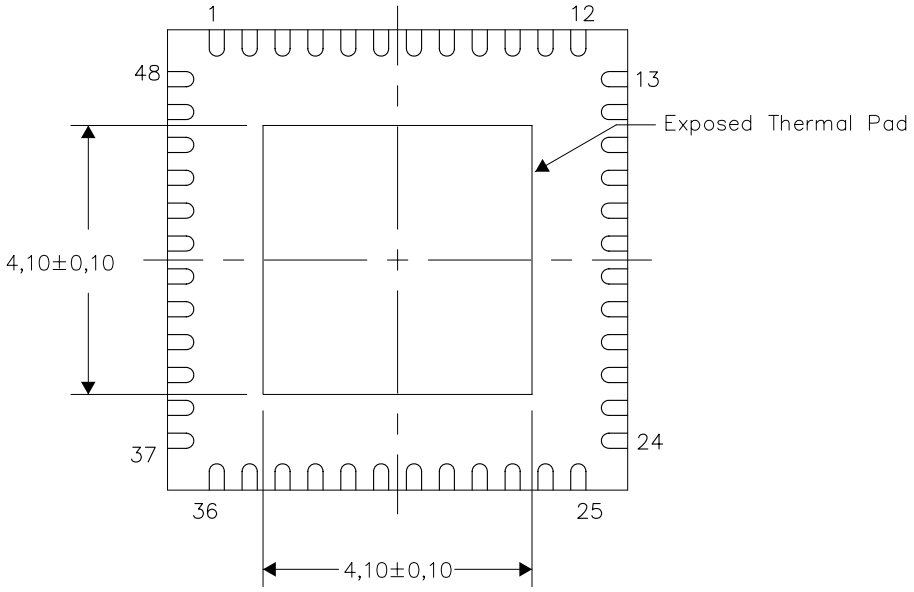
RGZ (S–PVQFN–N48)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

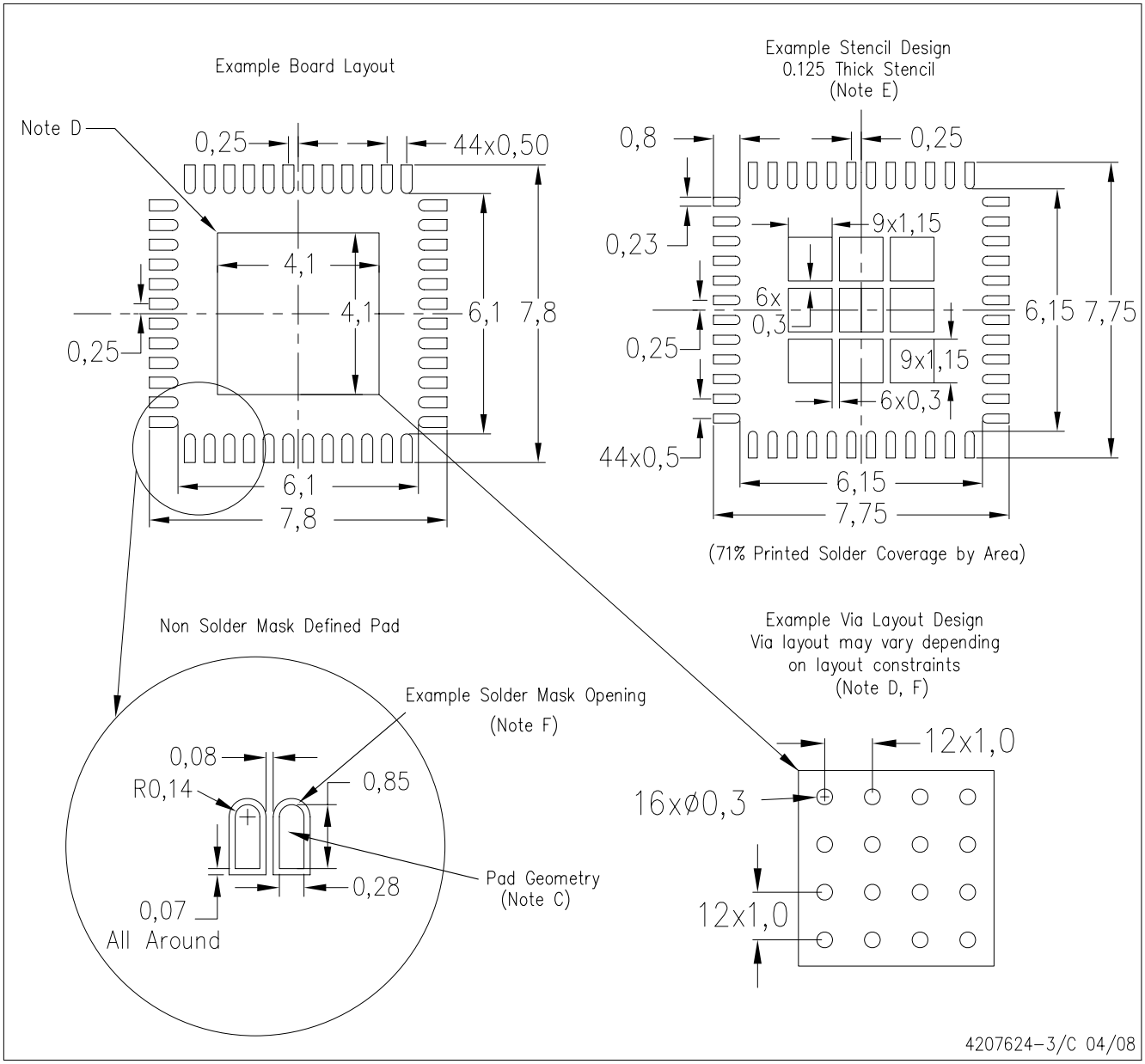


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGZ (S–PVQFN–N48)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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